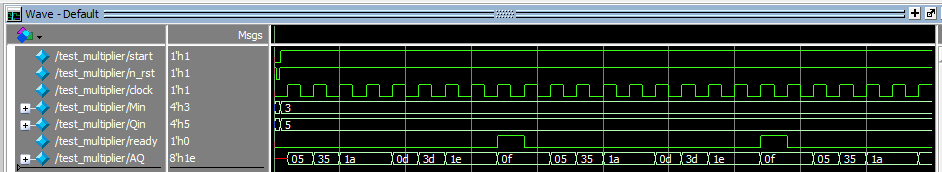
**M4 Lab si3g19**

**SystemVerilog and FPGAs**

3 Laboratory Work

3.1 RTL Simulation

Appropriate waveforms from ModelSim:

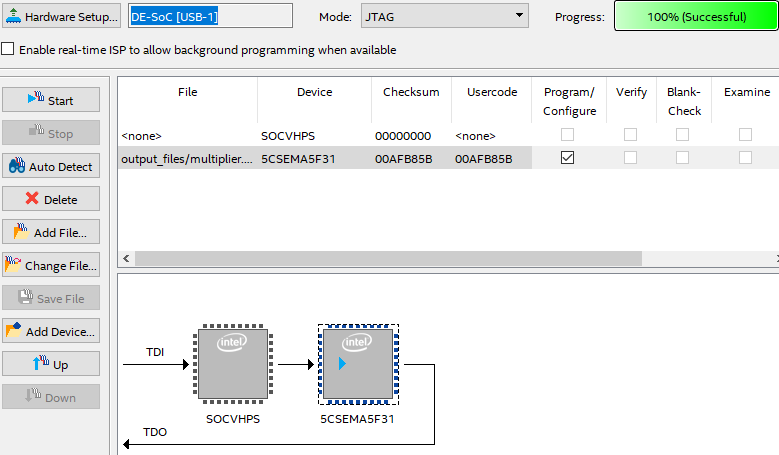


START signal Multiplier Q Multiplicand M

Product of M and Q, held in registers A and Q, once the active high output READY is asserted

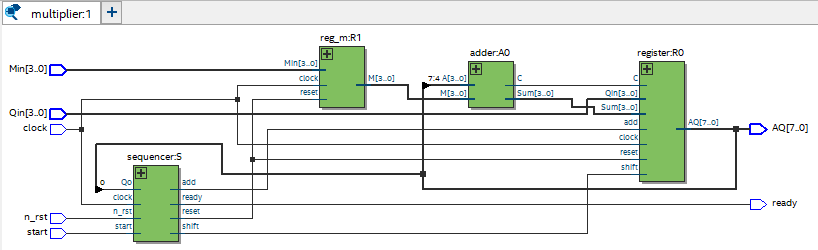
3.2 FPGA Synthesis

1. Design successfully downloaded onto FPGA



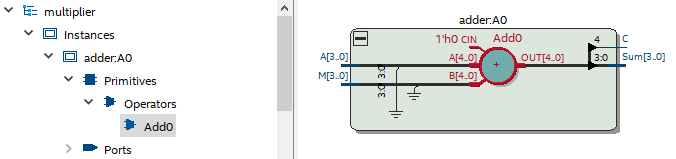
1. Schematic of your design from the RTL viewer in Quartus

Multiplier:

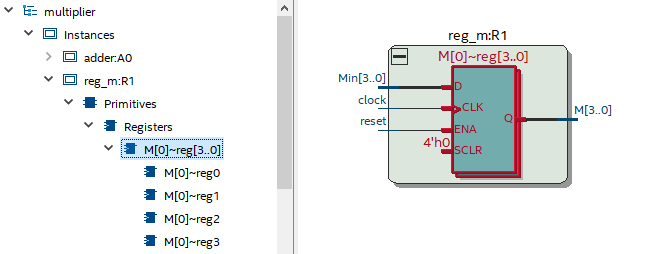


Instances:

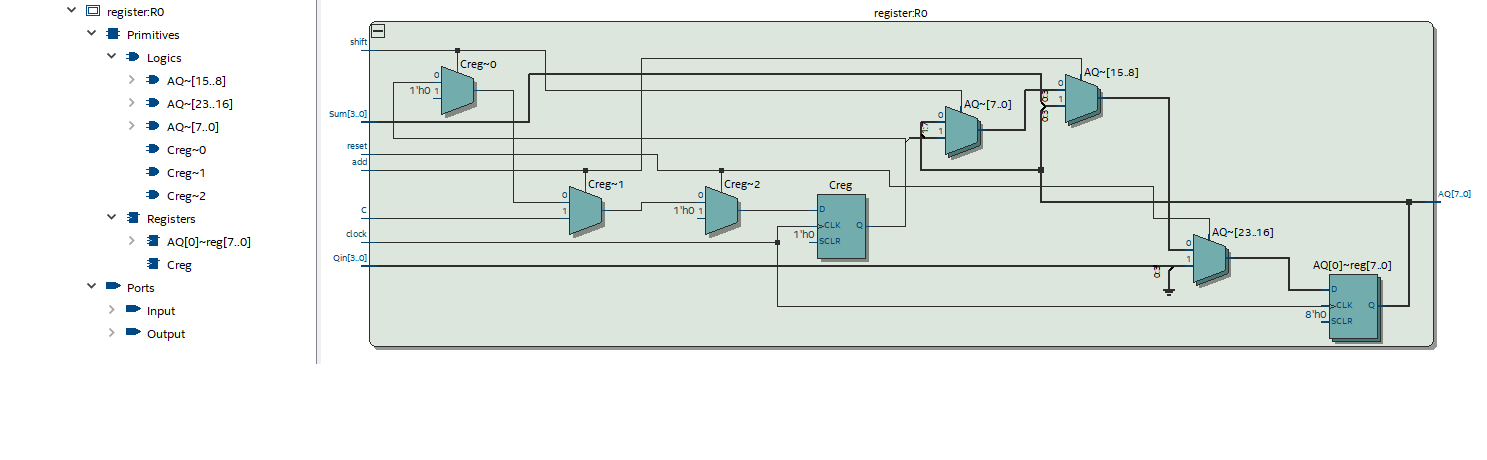
* Adder A0



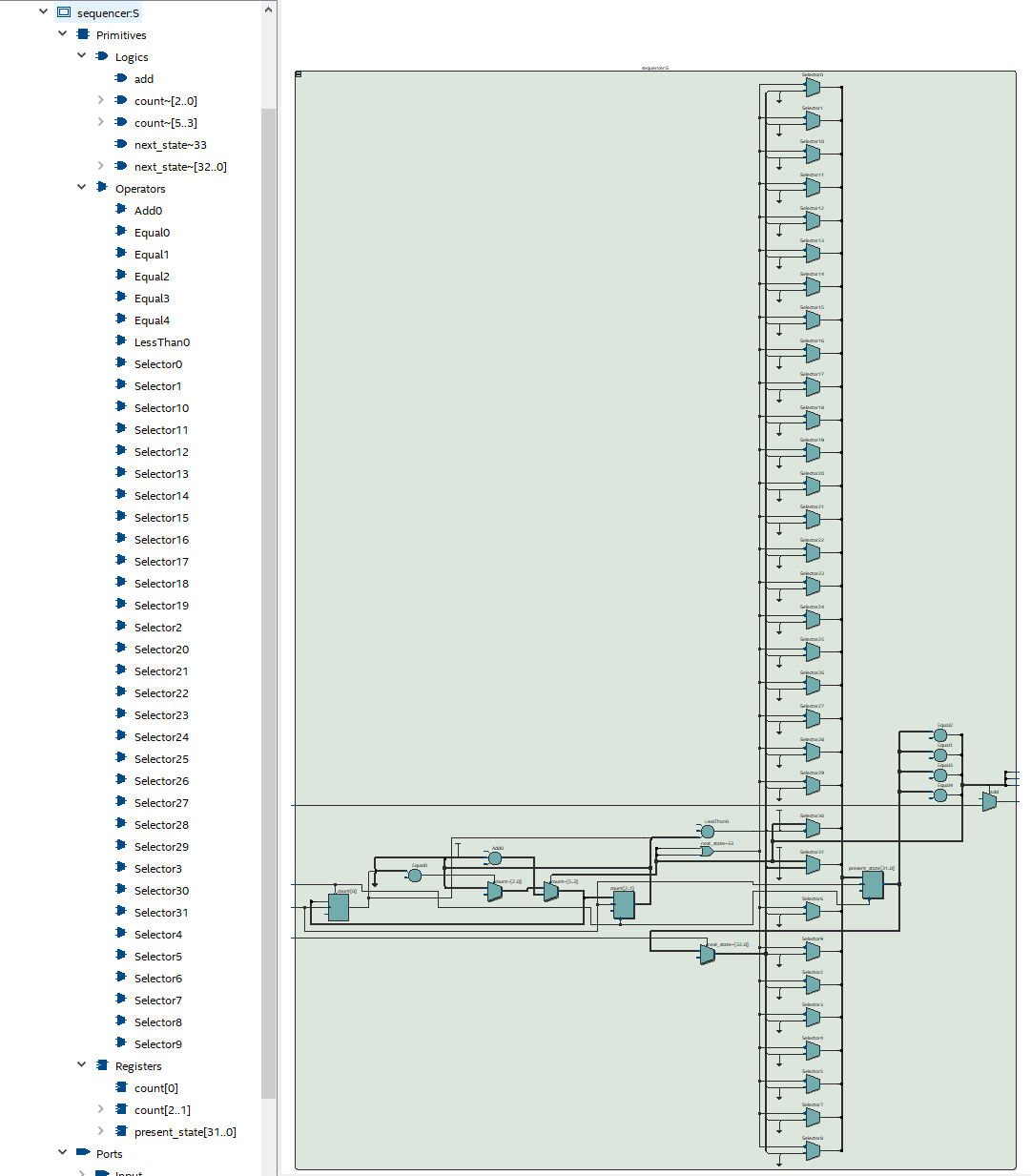
* Reg\_m R1



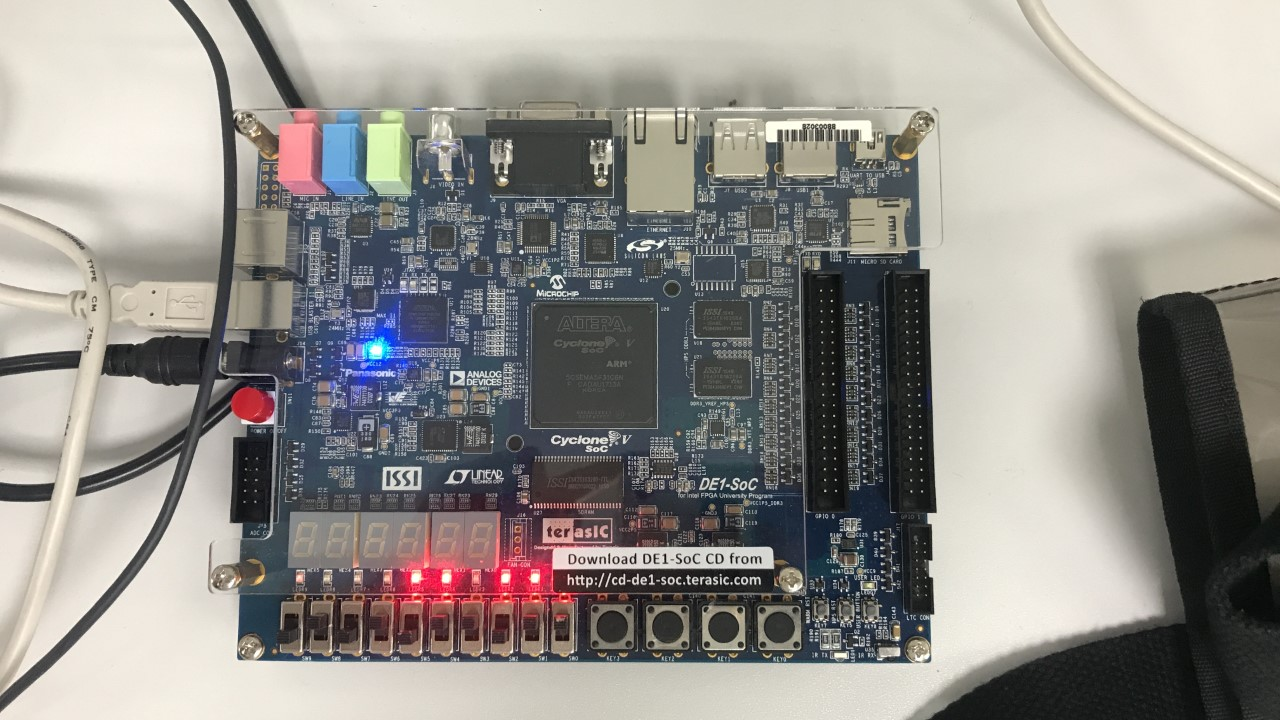
* Register R0



* Sequencer S



Testing:



Gave a cycle of

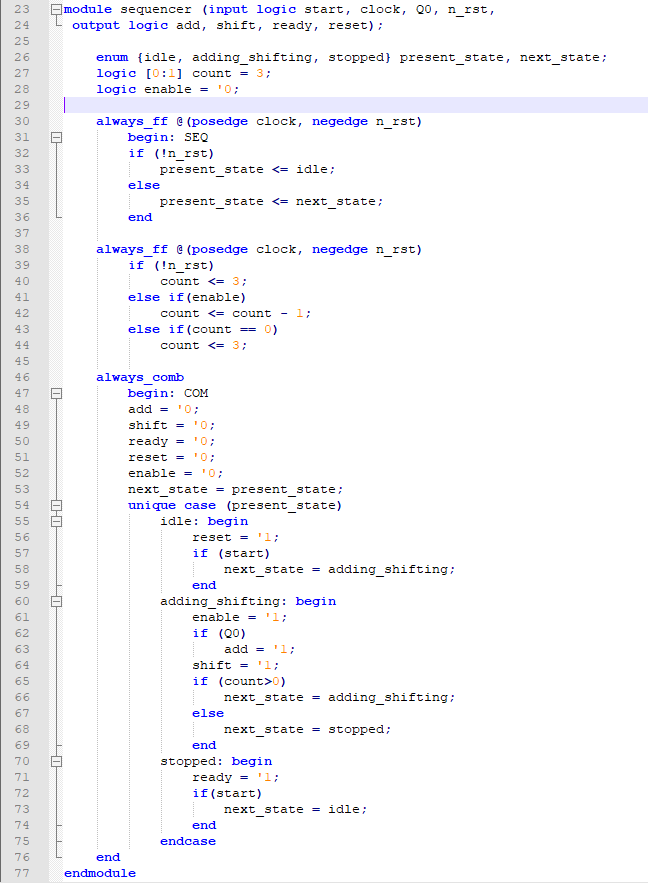
* 0100110111
* 0000110111
* 0000000101
* 0010110101
* 0001011010
* 0001011010
* 0000101101
* 0000101101
* 0011011101
* 0001101110
* 0001101110
* 0100110111

3.3 extended behaviour

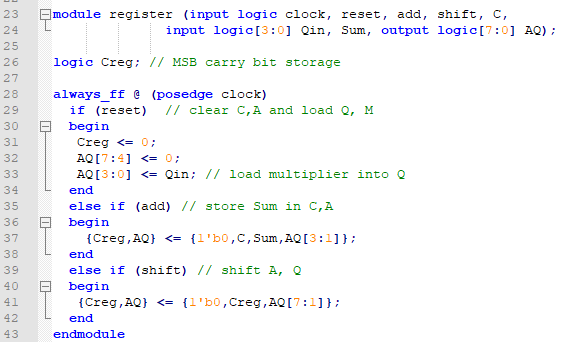
Combining the states ‘adding’ and ‘shifting’ into a single state 🡪‘adding\_shifting’#

Modifying ‘sequencer.sv’ and ‘register.sv’

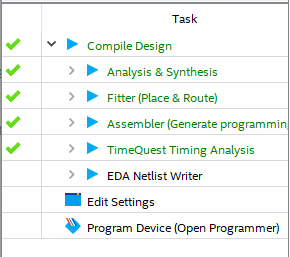
Sequencer.sv:



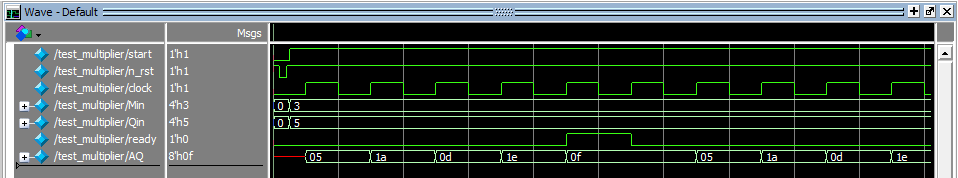
Register.sv:



Analysing and compiling code:



Modelsim waveform:



I successfully downloaded the design onto the FPGA as before and confirmed the behaviour by entering numbers and observing the LEDs on the board.